(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon layers in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said first polysilicon layer to thereby form a control gate and a floating gate;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

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(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said word lines and connecting source regions to one another and a plurality of bit studs extending to said drain regions;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a bit line extending perpendicularly to said word lines and connecting said drain regions with each other, said bit line having a top portion and a bottom portion with said top portion being wider than said bottom portion,

wherein said bottom portion of said bit line is connected to said top portion of said plurality of bit studs and said bottom portion of said plurality of bit studs is connected to said drain regions.

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24. (Amended) A method of fabricating an EEPROM semiconductor device, comprising the steps of:

(a) forming a plurality of field insulating films in parallel with one another and perpendicular to a plurality of word lines on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon layers in parallel with one another perpendicularly to said plurality of word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said first polysilicon layer to thereby form a control gate and a floating gate;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(h) forming a first metal wiring layer which is patterned so as to form both a bit line connecting said drain regions to one another, and a plurality of source studs extending in parallel with said word lines, said plurality of source studs connecting to said source regions, said plurality of source studs having a top portion and a bottom portion with said top portion of said plurality of source studs being wider than said bottom portion of said plurality of source studs;

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(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions with each other, said common source line having a top portion and a bottom portion with said top portion of said common source line being wider than said bottom portion of said common source line,

wherein said bottom portion of said common source line is connected to said top portion of said plurality of source studs and said bottom portion of said plurality of source studs is connected to said source regions.